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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,174	12/03/2001	S. Brandon Keller	10014123-1	6179

7590 04/08/2005

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,174	KELLER ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to patent application S/N: 09/998174, filed on 12/03/2001. Claims 1-20 are pending in the application.

Drawings

The drawings filed on 12/03/2001 are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh et al, US patent no. 5,878,053.

As per claim 1, Koh discloses a method and system for simulation of power network and network analysis for testing IC designs with feature limitations very similar to the claimed invention. According to Koh, the power network analysis includes steps

Selecting at least a first net from a plurality of nets contained in the distributed IC design (Figs. 3, 9, cols. 4-5),

Performing power net transformation by analyzing RC circuit equivalent and reducing the RC net to prevent electromigration loss and to have a simpler circuit structure as claimed (cols. 4-6). Koh does not expressly disclose the claimed step of "compressing" the power net.

Practitioner in the art at the time of the invention was made would have found it obvious Koh power net reduction above implies the claimed compressing because the power net transformation reduces circuit complexity by a simpler circuit and such reduction above would include net compression as shown in Fig. 7 to maintain or preserve power characteristics of the circuit netlist (col. 5, line 8 to col. 6, line 54).

As per claim 2, Koh discloses connector points being selected for power net reduction transformation or compression by reducing resistors for instance (col. 5, line 8 to col. 6, line 20).

As per claim 3, Koh discloses a selected circuit within a netlist as claimed.

As per claim 4, Koh discloses a plurality of nets in an IC design, each net is within a power grid net and isolated by a connector (cols. 5 and 6) for power test and analysis.

As per claim 5, due to the similarity of claim 5 to claim 1 above, claim 5 is also rejected under the same rationale as set forth.

As per claims 6-7, Koh discloses the claimed limitations in cols. 4-6.

As per claims 8 and 9, Koh discloses a method and system for a power network simulation and network analysis for testing IC designs with feature limitations very similar to the claimed invention. According to Koh, the power network analysis includes steps

Selecting at least a first net from a plurality of nets contained in the distributed IC design, each net isolated from each other by a connector to form a power net (Figs. 3, 9, cols. 4-5),

Performing power net transformation by analyzing RC circuit equivalent and reducing the RC net to prevent electromigration loss, to have a simpler circuit structure, and preserve circuit connection as claimed (cols. 4-6). Koh does not expressly disclose the claimed step of "compressing" the power net.

Practitioner in the art at the time of the invention was made would have found it obvious Koh power RC net reduction above implies the claimed compressing because the power net transformation reduces circuit complexity by a simpler circuit and such reduction above would include net compression as shown in Fig. 7 to maintain or preserve power characteristics of the circuit netlist (col. 5, line 8 to col. 6, line 54).

As per claims 10-11, Koh discloses a power net connector, which would include the claimed limitations for forming and defining a circuit power net (cols. 4-5).

As per claim 12-13, Koh discloses current in each reduced power net as claimed.

As per claim 14, Koh discloses a computer program product for reducing a distributed power net in an integrated circuit for simulating and testing IC designs with feature limitations very similar to the claimed invention. According to Koh, the power network program product includes means:

Selecting at least a first net from a plurality of nets contained in the distributed IC design, each net isolated from each other by a connector to form a power net (Figs. 3, 9, cols. 4-5),

Performing power net transformation by analyzing RC circuit equivalent and reducing the RC net to analyze electromigration loss, to have a simpler circuit structure,

and preserve circuit connection as claimed (cols. 4-6). Koh does not expressly disclose the claimed step of "compressing" the power net.

Practitioner in the art at the time of the invention was made would have found it obvious Koh power RC net reduction above implies the claimed compressing because the power net transformation reduces circuit complexity by a simpler circuit and such reduction above would include net compression as shown in Fig. 7 to maintain or preserve power characteristics of the circuit netlist (col. 5, line 8 to col. 6, line 54).

As per claims 15-16, Koh discloses net connectors and power net reduction such as resistors reduction, equivalent capacitance as known in circuit analysis techniques.

As per claim 17, Koh discloses a method and system for power network simulation and network analysis for testing IC designs with feature limitations very similar to the claimed invention. According to Koh, the power network analysis includes steps

Selecting at least a first net from a plurality of nets contained in the distributed IC design, each net isolated from each other by a connector to form a power net (Figs. 3, 9, cols. 4-5),

Performing power net transformation by analyzing RC circuit equivalent and reducing the RC net to analyze electromigration loss, to have a simpler circuit structure, and preserve circuit connection as claimed (cols. 4-6). Koh does not expressly disclose the claimed step of "compressing" the power net.

Practitioner in the art at the time of the invention was made would have found it obvious Koh power RC net reduction above implies the claimed compressing because

the power net transformation reduces circuit complexity by a simpler circuit and such reduction above would include net compression as shown in Fig. 7 to maintain or preserve power characteristics of the circuit netlist (col. 5, line 8 to col. 6, line 54).

As per claim 18, Koh discloses a method and system for power network simulation and network analysis for testing IC designs with feature limitations very similar to the claimed invention. According to Koh, the power network analysis includes steps

Selecting at least a first net from a plurality of nets contained in the distributed IC design, each net isolated from each other by a connector to form a power net (Figs. 3, 9, cols. 4-5),

Performing power net transformation by analyzing RC circuit equivalent and reducing the RC net to prevent electromigration loss, to have a simpler circuit structure, and preserve circuit connection as claimed (cols. 4-6). Koh does not expressly disclose the claimed step of "compressing" the power net.

Practitioner in the art at the time of the invention was made would have found it obvious Koh power RC net reduction above implies the claimed compressing because the power net transformation reduces circuit complexity by a simpler circuit and such reduction above would include net compression as shown in Fig. 7 to maintain or preserve power characteristics of the circuit netlist (col. 5, line 8 to col. 6, line 54).

As per claim 19, Koh discloses current net analysis including uncompressing power net for gross current estimation in each net.

As per claim 20, Koh discloses current net and net connector in the IC design (cols. 4-5).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 4,916,627, issued to Hathaway, David, on Apr. 1990

2. US patent no. 5,682,320, issued to Khouja et al, on Oct. 1997

3. US patent no. 6,247,162 B1, issued to Fujine et al, on June 2001

4. US patent no. 6,536,024 B1, issued to Hathaway, David, on Mar. 2003

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Apr. 01, 2005

Thai Phan
Patent Examiner
Art Unit 2128